

2.4 GS/s Dual-Channel Arbitrary Waveform Generator

C Size VXI Instrument Module

Introduction

Building on thirty years of success developing state-of-the-art measurement solutions, Analogic introduces the most advanced broadband stimulus instrumentation available today.

Engineers and scientists who rely on ultra-high-performance arbitrary waveform generators can anticipate significant performance improvements from the new DBS 2050A.

Finally, an arbitrary waveform generator (AWG) possesses the power and flexibility to provide the right signals for your applications.

- ☐ Dramatically improve the quality of performance characterization testing on all kinds of electronic devices
- ☐ Generate arbitrary waveforms, including Pulse Pattern and Sinusoidal stimulus, over a frequency range of DC to 1.2 GHz with 8 bits of vertical resolution and over 60 dB of programmable gain and offset
- ☐ Synchronize dual outputs with a maximum time skew of ± 100 ps
- ☐ Produce rise/fall times of 400 ps
- ☐ Play back waveforms with sample rate jitter of less than 10 ps RMS
- ☐ Increase memory efficiency by over 100 times over conventional AWG designs by using the flexible waveform and sequence memory architecture
- ☐ Use waveform independent runtime parameters to change the output level and offset "on the fly"
- ☐ Preload up to 4096 unique waveforms in memory and seamlessly link them for playback (creating very long waveform playback periods), using Dynamic Waveform Sequencing
- ☐ Advance from one waveform to the next using conditional waveform repeat (loop) counts as well as internal or external trigger events.
- ☐ Generate precise standard waveforms: square, sine, positive and negative ramps, pulse, noise, triangle, positive and negative haversines, $\sin(x)/x$, and DC

Bring your next high-speed analog or mixed signal design to market faster while dramatically reducing errors or oversight in critical design verifications. The DBS 2050A is ideal for use on the production floor or in the laboratory.

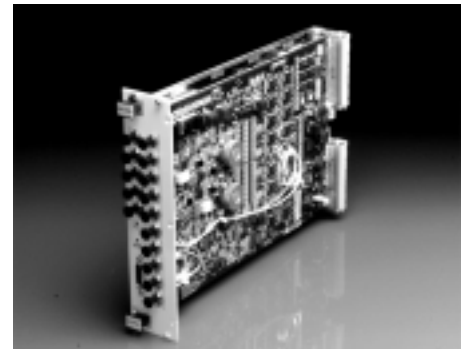
General Description

Analog signal outputs are available in true differential or single-ended form for one channel operation and single ended when operating in dual channel mode. Output amplitudes are 1.0V peak-to-peak using the primary X1 amplifiers; 4.0V peak-to-peak using the high-level X4 amplifiers. Offsets can be set to ± 3.5 V with 2 mV resolution.

In addition to the full bandwidth output, the DBS 2050A has three selectable low pass output filters with cutoff frequencies of 200 MHz, 20 MHz and 2 MHz.

Other filter requirements are accommodated with available SMA feed-thru filter modules.

The sampling clock is built around a precision phase detector capable of synchronizing to internal or external references. The sample clock rate is programmable over a range of 600 S/s to 2.4 GS/s. The external reference input can range from 2.5 MHz to 100 MHz.



Features

- ☐ Sampling Rate: 2.4 GS/s (Single Channel)
- ☐ Bandwidth: 800 MHz Typical
- ☐ Waveform Resolution: 8 Bit
- ☐ Voltage Range: 4.0V peak-to-peak
- ☐ Voltage Offset: ± 3.5 VDC
- ☐ Waveform Memory: 8 Mbytes
- ☐ Sequence Memory: 4k Segments
- ☐ 100% Performance Tested and Regulatory Certified
- ☐ Application Development:
 - VXI Plug and Play Compliant Drivers for WIN and Solaris Frameworks

Applications

- ☐ Automatic Test Equipment
- ☐ Telecommunications
- ☐ Mass Storage
- ☐ RADAR
- ☐ Ultrasonics
- ☐ Navigation
- ☐ LAN/WAN
- ☐ Wireless
- ☐ RF Controls

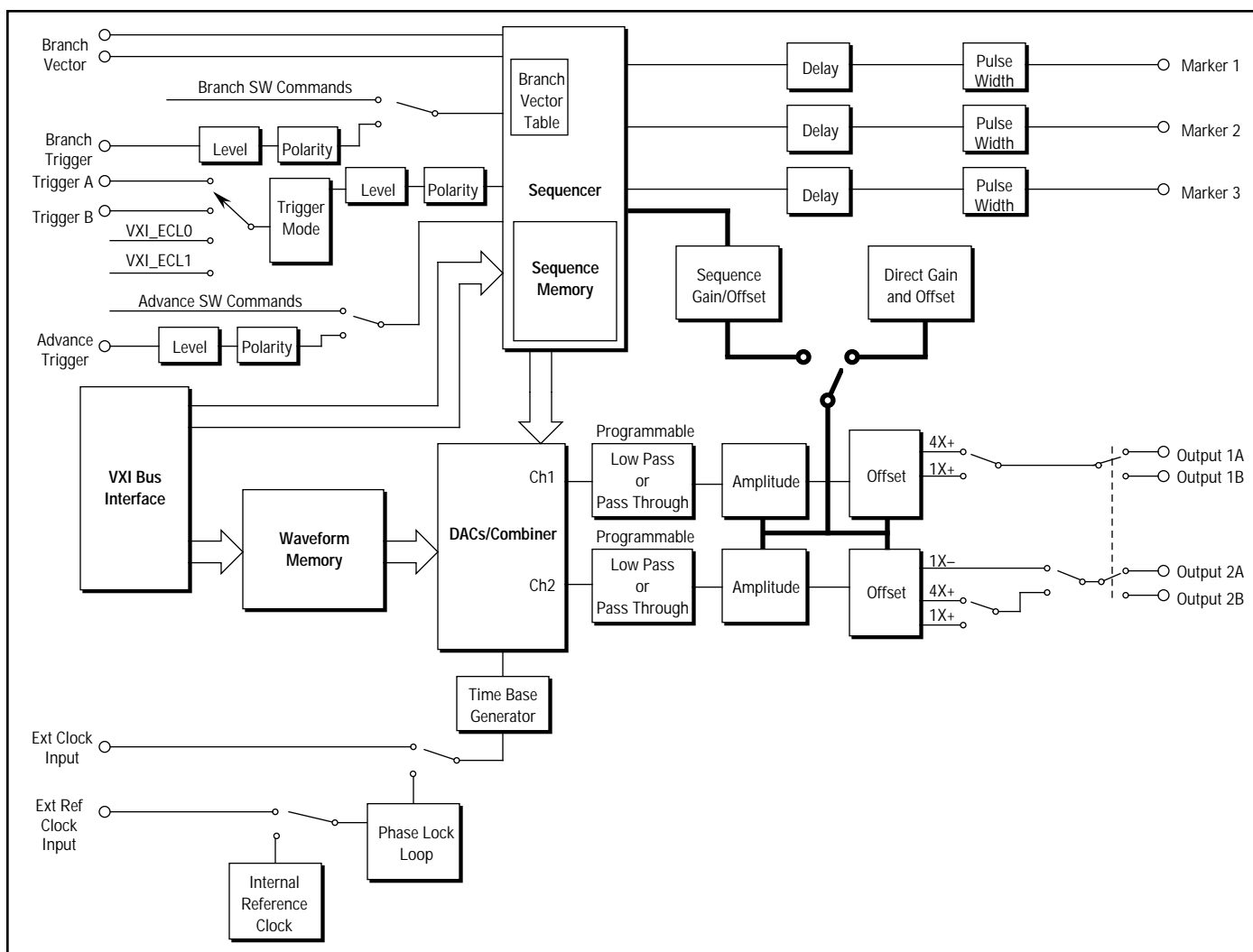


Figure 1. DBS 2050A Functional Block Diagram.

Flexible Operating Modes

Each output channel has two physical ports; A and B. This highly flexible architecture facilitates fast switching between ports without external control elements.

The high-level output amplifiers are capable of operation to 4.0V peak-to-peak. The low-level output amplifiers deliver 1.0V peak-to-peak waveforms with great spectral purity. Gain control has 60 dB of adjustment range.

Single Channel Modes

Mode	Main Output	Complementary Output
2.0 V Differential	1A 1B	2A 2B
1.0V Single Ended (X1 Output)	1A 1B	— —
4.0V Single Ended (X4 Output)	1A 1B	— —

Dynamic Waveform Sequencing

The unique architecture of the DBS 2050A provides a level of flexibility and functionality not found in any other arbitrary waveform generator.

Control of the output signal path is decoupled from waveform memory so gain and offset changes can be made over a wide dynamic range without disruption of the output signal.

Dual Channel Modes

Mode	Channel 1 Output	Channel 2 Output
1.0V Single Ended (X1 Output)	1A 1B	2A 2B
4.0V Single Ended (X4 Output)	1A 1B	2A 2B

VXI Bus Interface

The DBS 2050A comes equipped with a fully compliant VXI Plug and Play Driver, soft front panel and application source code. The toolset supports application-specific developments in Visual C/C++ or Visual BASIC, as well as National Instruments' LabWindows/CVI and LabVIEW.

Waveform creation and editing software is provided by Wavesmith™, a versatile waveform development system for Windows. This tool provides a "no programming required" work environment for rapid prototyping of user waveforms, as well as direct control of all instrument functions.

DBS 2050A

Specifications

OUTPUT CHARACTERISTICS		
Parameter	Conditions	Value
X1 OUTPUT MODE		
Max. Amplitude	Differential	2.0V pk-pk
	Single-Ended	1.0V pk-pk
Accuracy	50Ω Terminated	±2.0% at full scale
Gain Ctrl Accuracy	25° ±5°C	±1% of setting, ±.00025 V/V
Resolution		>3500 steps/60 dB
Flatness (1)	Sinusoid 0.5V pk-pk	±0.5 dB to 30 MHz
		±2.0 dB to 300 MHz
Bandwidth	<0.5V pk-pk	>700 MHz
Rise/Fall Time	<0.5V pk-pk	<500 ps
	<1.0V pk-pk	<600 ps
Amplitude Control Settling Time		50 ns to within 10% of final 200 ns to within 20% of final
X4 OUTPUT MODE		
Max. Amplitude	Single-Ended Only	4.0V p-p
Accuracy	50Ω Terminated	±2.0% at full scale
Gain Ctrl Accuracy	25° ±5°C	±1% of setting, ±.00025 V/V
Flatness (1)	Sinusoid 2.0V pk-pk	±0.5 dB to 30 MHz
		±2.0 dB to 100 MHz
Bandwidth	<2.0V pk-pk	>165.0 MHz
Rise/Fall Time	<2.0V pk-pk	<2.2 ns
	<4.0V pk-pk	<2.5 ns
DC OFFSET		
Resolution		2.0 mV
Range	Differential	±2.0V
	Single-Ended Mode	±3.5V
Accuracy Single-Ended Output	Output Mode (X1)	±2.0% of setting ±20 mV
	Output Mode (X4)	±2.0% of setting ±80 mV
Accuracy Differential Output	Common Mode X1 Output Mode	±2.0% of setting ±20 mV
	Differential X1 Output Mode	±2.0% of setting ±30 mV
Offset Control Settling Time		6 μs to within 2% of new setting Max.

SINEWAVE CHARACTERISTICS		
Parameter	Conditions	Value
X1 OUTPUT MODE		
SFDR		
<10 MHz	Measured from 1 MHz to Nyquist.	>45 dBc
<50 MHz		>40 dBc
<200 MHz	1.0V pk-pk 2.4 GS/s	>30 dBc
SINAD	50 MHz Carrier 1.0V pk-pk 2.4 GS/s 5 MHz to Nyquist	>37 dBc
X4 OUTPUT MODE		
SFDR		
<50 MHz	Measured from 1 MHz to 600 MHz 4.0V pk-pk 0V Offset	>40 dBc
SINAD	50 MHz Carrier 4.0V pk-pk 5 MHz to 605 MHz BW	37 dBc

FILTER CHARACTERISTICS		
Parameter	Conditions	Value
Type	3-pole Bessel Low Pass	
-3 dB Bandwidth	Selectable	2 MHz
		20 MHz
		200 MHz
Rise Time		0.35/Bandwidth

TIME BASE/SAMPLING CLOCK		
Parameter	Conditions	Value
INTERNAL SAMPLE CLOCK		
Range	Single Channel Mode	600 S/s to 2.4 GS/s
	Dual Channel Mode	300 S/s to 1.2 GS/s
Resolution		0.4% of Desired Rate Max.
Accuracy		±2 ppm Typ.
Jitter	100 ns Measurement Window Internal Clock Only	<10 ps RMS
EXTERNAL REFERENCE CLOCK INPUT		
Range	0.8 – 1.5V pk-pk	2.5 MHz to 100 MHz
Resolution	at	2.5 MHz Steps
Duty Cycle	10 MHz	50% Nom.
Impedance		50 ohms AC coupled
EXTERNAL SAMPLE CLOCK		
Range	0.8 – 1.5V pk-pk Slew Rate 0.5V/ns	100 kHz to 2.4 GHz

TRIGGER CHARACTERISTICS		
Parameter	Conditions	Value
MAIN TRIGGER		
Sources	Trigger A, Trigger B, ECL0, ECL1	
Modes	Free Run, Start, Stop, Gate and Start/Stop	
Threshold Range		±10.0V
Threshold Accuracy		±5% of Setting ±140 mV Typ.
Hysteresis		40 mV pk-pk
Input Impedance		4.0 kΩ Nom.
Trigger to Output Delay	Dual Channel Mode	42 ns + 17 clock cycles
	Single Channel Mode	42 ns + 35 clock cycles
BRANCH AND ADVANCE TRIGGER		
Threshold	TTL Mode	1.5V Typ.
	Zero Crossing	0V Typ.
Input Impedance		10 kΩ Nom.
Trigger to Output Delay		1.66 μs + 256/FS (2)

MARKER OUTPUTS 1, 2, 3		
Parameter	Conditions	Value
Output	No Load	TTL
Impedance		50Ω Nom.
Delay Range		0 to 2 x 10 ⁶ x sample clock period Max.
Delay Resolution		32 x sample clock period
Pulse Width Range		0 to 1.31 x 10 ⁵ x sample clock period Max.
Resolution Response		32 x sample clock period

PHYSICAL CHARACTERISTICS		
Parameter	Conditions	Value
Weight	Without Packaging	7.25 kg
Size		VXI Double Wide C Size
Cooling		7 liters/sec

REGULATORY	
VXI Compliance	VXI Plug and Play Register based instrument REV 1.4
Electromagnetic Compatibility	EN61326-1 Class A FCC Part 15, Subpart B, Class A
Safety	EN61010-1, IEC 1010-1, UL3111-1

DBS 2050A

Specifications (cont.)

ENVIRONMENTAL		
Parameter	Conditions	Value
Operating Temperature Range	At Rated Air Flow Full Compliance with Specifications	10°C to 40°C
Storage Temperature Range		-20°C to +70°C
Relative Humidity	Non-Condensing	10%–90%
Total Power Dissipation	Operating	130 watts
DC Current Consumption	+5 VDC	6.2A
	-5.2 VDC	8.5A
	+24 VDC	0.1A
	-24 VDC	0.1A
	+12 VDC	0.7A
	-12 VDC	1.0A
Vibration	Operating	IEC 68-2-6
	Non-Operating	
Shock	Operating	6.0G, 11 ms sine IEC 68-2-29
	Non-Operating	10G

CALIBRATION/WARRANTY	
Maintenance	Unit is self-calibrating at startup
Warm-Up Time	15 minutes
Recommended Factory Re-Certification	Annually

ACCESSORIES	
User's Manual	
Support Software	Includes: <ul style="list-style-type: none"> VXI P&P Driver for WIN NT, WIN 95, WIN 98 LabView Soft Front Panel Source Code Wavesmith™ Waveform Development Software for Win NT, 95, 98
Contact Analogic for a complete listing of other VXI products and accessories.	

Notes

All specifications are subject to change without notice.

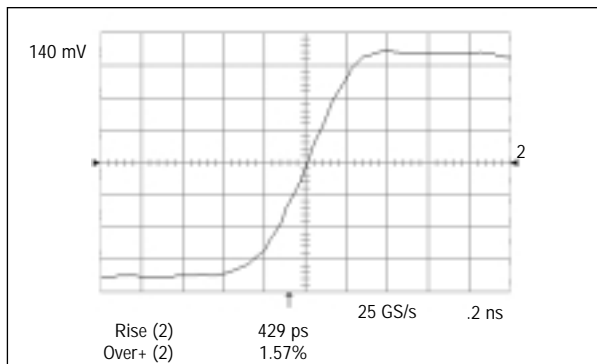
All specifications are valid within the operating limits stated.

Calibration values are not user accessible.

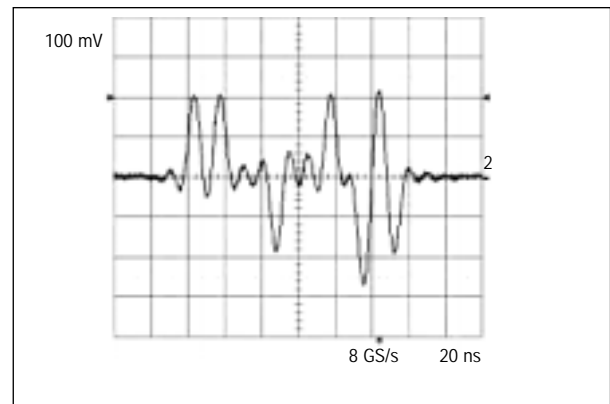
All specifications are valid for 50Ω output terminations unless otherwise stated.

1. Allowance Made for sin(x)/x Rolloff.

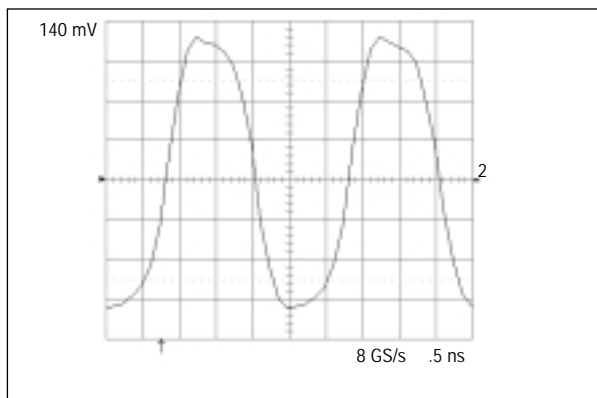
2. FS — sample clock rate.



Typical rise time -FS to +FS in one sample clock period.



Typical PR4 pulse pattern. 6 ns step size. 10 pts/bit pulse.



Square wave, 6 pts/cycle. Sampled at 2.4 GS/s.